AMENDMENT TO THE CLAIMS

1-5 (Cancelled)

6. (Original) A method of scheduling an instruction to a processor having a plurality of memory cache banks, comprising:

predicting which of the plurality of memory cache banks is associated with the instruction; and

assigning the instruction for execution to one of the plurality of cache memory banks based on the predicted memory cache bank.

7. (Original) The method of claim 6, wherein said predicting is based on information related to at least one of: (i) a bank history; (ii) a control flow information; and (iii) a load target-address information.

8. (Original) The method of claim 6, wherein said predicting comprises performing a plurality of binary evaluations and the prediction is based on a majority vote of the plurality of binary evaluations.

9. (Original) The method of claim 6, wherein said predicting comprises a plurality of evaluations, each evaluation being associated with a confidence, and the prediction is based on the plurality of evaluation confidences.

10. (Original) The method of claim 9, wherein said predicting is based on a sum of evaluation confidences above a threshold value.

11. (Currently Amended) An article of manufacture including a computer-readable medium having stored thereon instructions, ~~adapted to be~~ which when executed by a processor ~~having a plurality of memory cache banks to implement a method to~~ cause the processor to ~~schedule an instruction, the~~ perform a method comprising:

predicting which of ~~the~~ a plurality of memory cache banks is associated with ~~the~~ an instruction; and

assigning the instruction for execution to one of the plurality of cache memory banks based on the predicted memory cache bank.

12. (Currently Amended) A processor ~~having a first memory cache bank and a second memory cache bank~~, comprising:

a first memory cache bank;

a second memory cache bank;

a memory cache bank prediction unit to predict which of the plurality of memory cache banks is associated with an instruction; and

a scheduler coupled to said memory cache bank prediction unit ~~and~~ to assign the instruction for execution to one of the plurality of cache memory banks based on the predicted memory cache bank.

13. (Currently Amended) A processor ~~having a first memory cache bank and a second memory cache bank~~, comprising:

a first memory cache bank;

a second memory cache bank;

a memory cache bank prediction unit;

a scheduler coupled to said memory cache bank prediction unit;

a first instruction pipeline ~~between said~~ coupled to the scheduler and the first memory cache bank; and

a second instruction pipeline ~~between said~~ coupled to the scheduler and the second memory cache bank;

wherein an instruction is ~~placed~~ to be scheduled for execution in both said first instruction pipeline and said second instruction pipeline by the scheduler in response to a prediction by the memory cache bank prediction unit.

14. (Original) The processor of claim 13, wherein instructions in the first pipeline are unable to access information in the second memory cache bank and instruction in the second pipeline are unable to access information the first memory cache bank.

15. (Original) The processor of claim 14, wherein an instruction in the first instruction pipeline is discarded if it needs to access information in the second memory cache bank.

16. (Original) The processor of claim 13, wherein said prediction unit predicts based on information related to at least one of: (i) a bank history; (ii) a control flow information; and (iii) a load target-address information.

17. (Original) The processor of claim 13, wherein said prediction unit performs a plurality of binary evaluations and the prediction is based on a majority vote of the plurality of binary evaluations.

18. (Original) The processor of claim 13, wherein said prediction unit performs a plurality of evaluations, each evaluation being associated with a confidence, and the prediction is based on the plurality of evaluation confidences.

19. (Original) The processor of claim 18, wherein said prediction unit predicts based on a sum of evaluation confidences above a threshold value.

20. (Currently Amended) A method ~~of executing an instruction in a processor having (i) a first instruction pipeline between a scheduler and a first memory cache bank and (ii) a second instruction pipeline between the scheduler and a second memory cache bank~~, comprising:

making a prediction which of a first memory cache bank and a second memory cache bank is associated with an instruction; and

processing an instruction in both a first instruction pipeline coupled to a scheduler and the first memory cache bank and a second instruction pipeline coupled to the scheduler and the second memory cache bank in response to the prediction.

~~predicting which of the memory cache banks is associated with the instruction; and~~

~~processing the instruction in both the first instruction pipeline and the second instruction pipeline in response to the prediction.~~

21. (Currently Amended) An article of manufacture including a computer-readable medium having stored thereon instructions, which when executed by a processor ~~having (i) a first instruction pipeline between a scheduler and a first memory cache bank and (ii) a second instruction pipeline between the scheduler and a second memory cache bank to implement a method to~~ cause the processor to ~~execute an instruction, the~~ perform a method comprising:

making a prediction which of a first memory cache bank and a second memory cache bank is associated with an instruction; and

processing an instruction in both a first instruction pipeline coupled to a scheduler and the first memory cache bank and a second instruction pipeline coupled to the scheduler and the second memory cache bank in response to the prediction.

~~processing the instruction in both the first instruction pipeline and the second instruction pipeline in response to the prediction.~~

22. (New) The article of manufacture of claim 11, the method further comprising:

performing a plurality of binary evaluations; and

predicting which of the plurality of memory cache banks is associated with the instruction based on a majority vote of the plurality of binary evaluations.

23. (New) The article of manufacture of claim 11, the method further comprising:

performing a plurality of evaluations, each evaluation being associated with a confidence; and

predicting which of the plurality of memory cache banks is associated with the instruction based on the plurality of evaluation confidences.

24. (New) The article of manufacture of claim 23, the method further comprising predicting which of the plurality of memory cache banks is associated with the instruction based on a sum of evaluation confidences above a threshold value.

25. (New) The processor of claim 12, wherein the memory cache bank prediction unit performs a plurality of binary evaluations and predicts which of the plurality of memory cache banks is associated with the instruction based on a majority vote of the plurality of binary evaluations.

26. (New) The processor of claim 12, wherein:

the memory cache bank prediction unit performs a plurality of evaluations, each evaluation being associated with a confidence; and

the memory cache bank prediction unit predicts which of the plurality of memory cache banks is associated with the instruction based on the plurality of evaluation confidences.

27. (New) The processor of claim 26, wherein the memory cache bank prediction unit predicts which of the plurality of memory cache banks is associated with the instruction based on a sum of evaluation confidences above a threshold value.

28. (New) The method of claim 20, further comprising:

performing a plurality of binary evaluations; and

basing the prediction on a majority vote of the plurality of binary evaluations.

29. (New) The method of claim 20, further comprising:

performing a plurality of evaluations, each evaluation being associated with a confidence; and

basing the prediction on the plurality of evaluation confidences.

30. (New) The method of claim 29, further comprising basing the prediction on a sum of evaluation confidences above a threshold value.

31. (New) The article of manufacture of claim 21, the method further comprising:

performing a plurality of binary evaluations; and

basing the prediction on a majority vote of the plurality of binary evaluations.

32. (New) The article of manufacture of claim 21, the method further comprising:

performing a plurality of evaluations, each evaluation being associated with a confidence; and

basing the prediction on the plurality of evaluation confidences.

33. (New) The article of manufacture of claim 32, the method further comprising basing the prediction on a sum of evaluation confidences above a threshold value.